UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,479	03/12/2004	Kenneth Hubbard	CIS03-68(8178)	8394

47654 7590 07/24/2006

DAVID E. HUANG, ESQ.
BAINWOOD HUANG & ASSOCIATES LLC
2 CONNECTOR ROAD
SUITE 2A
WESTBOROUGH, MA 01581

EXAMINER	
KUNZER, BRIAN	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 07/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,479	HUBBARD ET AL.	
	Examiner	Art Unit	
	Brian Kunzer	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) (amendment) filed on *13 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 13,15-18,20, and 29 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 13,15-18,20, and 29 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Amendments

The request for continued examination, filed June 13th, 2006 has been received and entered. In summary, claims 1-12, 14, 19, and 21-28 have been cancelled, claim 13 has been amended, and new claim 29 has been added, thus claims 13, 15-18, 20, and 29 are now pending examination.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

1. Claim 13 and claims 15-18, 20 and 29 (dependent therefrom) are rejected under 35 U.S.C. 101 because the limitations from claims 13 and 29 are not drawn to any of the patentable inventions described above. Instead the limitations are simultaneously drawn to a process and a manufacture (commonly known as process of making a product and product made), which is not a patentable invention. See MPEP § 2173.05(p).

Specifically, the following limitations of claims 13 and 29 are drawn to a process of making:

IN CLAIM 13:

A method for manufacturing an area array package comprising:

coupling a grid array of primary electrical contacts to a coupling surface of a substrate within a central portion defined by the substrate, the grid array of primary electrical contacts configured to carry at least data signals between the area array package and a circuit board;

forming the primary electrical contacts of the grid array as a plurality of primary solder balls, each primary solder ball of the grid array defining a first diameter;

coupling a series of secondary electrical contacts to the coupling surface of the substrate within a peripheral area defined by the coupling surface, the series of secondary electrical contacts configured to carry power signals between the area array package and the circuit board, the series of secondary electrical contacts separate from the grid array;

forming the series of secondary electrical contacts as a plurality of secondary solder balls, each secondary solder ball of the series defining a second diameter, the second diameter defined by each of the secondary solder balls being greater than the first diameter defined by each of the primary solder balls;

wherein coupling the series of secondary electrical contacts comprises coupling the series of secondary electrical contacts to the coupling surface of the substrate, the coupling surface configured to oppose a mounting surface of the circuit board.

IN CLAIM 29:

The method of claim 13 further comprising surface mounting a die to a second surface of the substrate, the second surface of the substrate opposing the coupling surface of the substrate, to electrically couple the die with the first set of contact pads and the second set of contact pads.

Additionally, the following limitations of claims 13 and 29 are drawn to a product and constitute mere structural limitations that do not affect the process of making in a manipulative sense:

IN CLAIM 13:

the substrate having at least one power plane, at least one ground plane, at least one plated through hole in communication with the at least one power plane, and at least one plated through hole in communication with the ground plane;

the substrate having a contact pad in electrical communication with the at least one plated through hole in communication with the at least one power plane and electrically coupled with a secondary solder ball of the series of secondary electrical contacts;

the substrate having a contact pad in electrical communication with the at least one plated through hole in communication with the at least one ground plane and electrically coupled with a secondary solder ball of the series of secondary electrical contacts;

the secondary solder ball, contact pad, and the at least one plated through hole in communication with the at least one power plane configured to carry power to the at least one power plane through the coupling surface; and

the secondary solder ball, contact pad, and the at least one plated through hole in communication with the at least one ground plane configured to carry power from the at least one ground plane through the coupling surface.

IN CLAIM 29:

wherein the die is configured to exchange, through second surface of the substrate, at least data signals with the circuit board through the grid array of primary electrical contacts and wherein the die is configured to exchange, through second surface of the substrate, power signals with the circuit board via the at least one secondary solder ball, the at least one contact pad, and the at least one plated through hole.

2. The Applicant must limit the invention to a process ***or*** a manufacture (product) as disclosed in section 35 U.S.C. 101. Accordingly, since Applicant has already elected, in the reply filed August 29th, 2005, the invention associated with the process/method of making the device, as detailed in restriction requirement mailed August 10th, 2005, the claims and limitations therein should be directed to the method of making the device. **Therefore, the above outlined product limitations must be removed from claims 13 and 29 to overcome this rejection.**

3. Note well, in regards to these limitations, that it has been held that to be entitled to weight in method claims, the recited-structure limitations therein must affect the method in a manipulative sense, and not to amount to the mere claiming of a use of a particular structure. Ex parte Pfeiffer, 1962 C.D. 408 (1961).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 13, 15-18, 20, and 29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 13 and 29 are ambiguous in the respect that they contain product structural limitations in addition to process/method limitations - **as outlined above under the 35 U.S.C. 101 rejection** - and therefore do not define a definite or patentable invention. See MPEP § 2173.05(p). Note Ex parte Lyell, 17 USPQ2d 1548 (Bd. Pat. App. & Inter. 1990). **Accordingly, the above outlined product limitations must be removed from claims 13 and 29 to overcome this rejection.**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 13, 15, 18, 20, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jackson (US Patent No. 6,627,822) in view of Byun (US Patent No. 6,736,306).

With respect to claim 13, Jackson teaches, from figs. 1A-1D and 5, the method for manufacturing an area array package comprising:

coupling a grid array of primary electrical contacts (120) to a coupling surface of a substrate (108) within a central portion defined by the substrate, the grid array of primary

electrical contacts (120) configured to carry at least data signals between the area array package (108) and a circuit board (101) (see column 4, lines 6-12);

forming the primary electrical contacts as a plurality of solder balls (114), each primary solder ball of the grid array defining a first diameter;

coupling a series of secondary electrical contacts (110) to the coupling surface of the substrate (108) within a peripheral area defined by the coupling surface, the series of secondary electrical contacts configured to carry power signals between the area array package (108) and the circuit board (101) (see column 4, lines 2-6), the series of secondary electrical contacts (110) separate from the grid array;

wherein coupling the series of secondary electrical contacts (110) comprises coupling the series of secondary electrical contacts (110) to the coupling surface of the substrate (108), the coupling surface configured to oppose a mounting surface of the circuit board (101).

However, Jackson does not teach forming the series of secondary electrical contacts as a plurality of secondary solder balls, each secondary solder ball of the series defining a second diameter, the second diameter defined by each of the secondary solder balls being greater than the first diameter defined by each of the primary solder balls. Instead, Jackson teaches the use of pins as the secondary electrical contacts.

Byun, drawn to ball grid array design for flip chips, does teach, from figs. 5 and 6, forming the series of secondary electrical contacts as a plurality of secondary solder balls (162), each secondary solder ball of the series defining a second diameter, the second diameter defined by each of the secondary solder balls being greater than the first diameter defined by each of the primary solder balls (160).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to create the device of Jackson utilizing the ball grid array of Byun as this would simply replace the pins of Jackson with larger diameter solder balls which still has the same desired effect as described by Jackson to create,

> "an electronic assembly for making power and signal connections between two substrates or between a semiconductor chip, socket or other device and a circuit board or the like that separates the power and signal connections, utilizes the appropriate type of connection and size and shape connection for the function being performed, makes efficient use of available area for making power and signal connections by minimizing the area on the chip or die and on the circuit board needed for making power and signal connections, and may be made efficiently with compatible manufacturing techniques or processes to form both the power and signal connections." (column 2, lines 2-13)

6. Additionally, the following limitations in claim 13 are drawn to a product and constitute mere structural limitations that do not affect the process of making in a manipulative sense - see Ex parte Pfeiffer, 1962 C.D. 408 (1961) - thus, they will not be given patentable weight:

"the substrate having at least one power plane, at least one ground plane, at least one plated through hole in communication with the at least one power plane, and at least one plated through hole in communication with the ground plane;

the substrate having a contact pad in electrical communication with the at least one plated through hole in communication with the at least one power plane and electrically coupled with a secondary solder ball of the series of secondary electrical contacts;

the substrate having a contact pad in electrical communication with the at least one plated through hole in communication with the at least one ground plane and electrically coupled with a secondary solder ball of the series of secondary electrical contacts;

the secondary solder ball, contact pad, and the at least one plated through hole in communication with the at least one power plane configured to carry power to the at least one power plane through the coupling surface; and

the secondary solder ball, contact pad, and the at least one plated through hole in communication with the at least one ground plane configured to carry power from the at least one ground plane through the coupling surface."

With respect to claim 15, Jackson, from fig. 5, and Byun, from fig. 8c, teaches the method wherein the step of forming the series of secondary electrical contacts (pins of Jackson or second set of solder balls of Byun) comprises:

placing at least two solder balls on a contact pad oriented within the peripheral area defined by the coupling surface, each solder ball defining a first diameter,

heating the at least two solder balls to cause the solder to undergo reflow (see column 5, lines 16-18 of Byun)

forming a secondary solder ball on the contact pad, secondary solder ball of the [series] defining a second diameter, the second diameter defined by the secondary solder ball being greater than the first diameter defined by each of the primary solder balls.

With respect to claim 18, Jackson, combined with Byun, discloses all the limitations except for specifically teaching the method wherein the substrate defines a length of at least approximately 60 mm and a width of at least approximately 60 mm. It would have been obvious to have a substrate with the dimensions of 60mm X 60mm, since such a modification would have

involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955).

Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669,149 USPQ 47 (CCPA 1966). Note also that it has been held that to be entitled to weight in method claims, the recited-structure limitations therein must affect the method in a manipulative sense, and not to amount to the mere claiming of a use of a particular structure. Ex parte Pfeiffer, 1962 C.D. 408 (1961).

With respect to claim 20, Jackson, combined with Byun, discloses all the limitations except for specifically teaching the method wherein the grid array of primary solder balls is configured in an array pattern of 50 columns having 50 primary solder balls per column. It would have been obvious to have a 50 X 50 grid array, since such a modification would have involved a mere change in the size of a component wherein the number of solder balls could easily be changed with a change in solder ball diameter or substrate area. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955).

Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected

result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669,149 USPQ 47 (CCPA 1966). Note also that it has been held that to be entitled to weight in method claims, the recited-structure limitations therein must affect the method in a manipulative sense, and not to amount to the mere claiming of a use of a particular structure. Ex parte Pfeiffer, 1962 C.D. 408 (1961).

With respect to claim 29, Jackson teaches, from figs. 1A-1D and 5, the method further comprising surface mounting a die (chip) to a second surface of the substrate (socket), the second surface of the substrate (socket) opposing the coupling surface of the substrate, to inherently electrically couple the die (chip) with the first set of contact pads and the second set of contact pads. (See column 2, lines 64-67.)

7. Additionally, the following limitations in claim 29 are drawn to a product and constitute mere structural limitations that do not affect the process of making in a manipulative sense - see Ex parte Pfeiffer, 1962 C.D. 408 (1961) - thus, they will not be given patentable weight: "wherein the die is configured to exchange, through second surface of the substrate, at least data signals with the circuit board through the grid array of primary electrical contacts and wherein the die is configured to exchange, through second surface of the substrate, power signals with the circuit board via the at least one secondary solder ball, the at least one contact pad, and the at least one plated through hole."

8. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jackson (US Patent No. 6,627,822) and Byun (US Patent No. 6,736,306) as applied to claim 13 and 21 above, and further in view of Barber (US Patent No. 6,600,220).

With respect to claim 16, Jackson and Byun teach the method described above.

Jackson and Byun do not specifically teach the coupling of at least one power regulation device to the substrate and in electrical communication with the series of secondary electrical contacts.

Barber, drawn to power distribution in multi-chip modules, teaches, from fig. 1A, coupling a plurality of voltage converters (42) (i.e. a power regulation device) to a substrate (28) in communication with the power supply lines (34) (i.e. series of secondary electrical contacts).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to create the device of Jackson coupled with the power regulation scheme of Barber permitting "the multi-chip module (MCM) to receive power at higher voltages than is supported by the high-density thin-film circuit region, decreasing MCM input current magnitudes and reducing noise and energy losses." (abstract of 6,600,220)

9. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jackson (US Patent No. 6,627,822) and Byun (US Patent No. 6,736,306) as applied to claim 13 and 21 above, and further in view of Amir (US Patent No. 6,787,920).

With respect to claim 17, Jackson, combined with Byun, discloses all the limitations except for specifically teaching that the method comprises coupling the plurality of secondary solder balls to the substrate at a pitch of at least approximately 5 mm.

However integrated circuit (IC) package designers take into account several design parameters when deciding on the dimension for the pitch (i.e. the interval spacing of the contacts), including the well-known problem of bridging. Bridging occurs during the solder reflow process in which two separate contacts will merge together and short out the circuit because there is a too fine of a pitch. (See column 1, line 66 – column 2, line 8 of Amir.)

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the combined device of Jackson and Byun and have the appropriately sized pitch, such as 5mm, in order to reduce the bridging effect as disclosed by Amir because this specific dimension is the result of finding an optimized parameter for a well known problem which is typically accounted for in all similar devices; and a change in size and discovering an optimum value of a result effective variable is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955). In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Response to Arguments

10. Applicant's arguments filed on June 13th, 2006 with respect to claims 13, 15-18, 20, and 29 have been considered but are not persuasive, but more importantly are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Kunzer whose telephone number is (571) 272-5054. The examiner can normally be reached on Monday-Friday 8:00-4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BK
7/14/2006

ANH D. MAI
PRIMARY EXAMINER